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Amendments to the Claims

Please amend Claims 3, 9, 14, 22, 26, 33, 37, 42, 46, 59, 67, 71, 74, 102 and 114 as follows:

1. (Previously Presented) A circuit, comprising:
  - a) a differential signal transmission line;
  - b) a common mode circuit comprising first and second resistances in series, said common mode circuit in communication with said differential signal transmission line, configured to reduce a swing of said differential signal transmission line; and
  - c) at least one overvoltage protection circuit in communication with said common mode circuit, wherein at least part of said common mode circuit is electrically interposed between said overvoltage protection circuit and said differential signal transmission line.
2. (Previously Presented) The circuit of Claim 18, wherein said common mode circuit comprises first and second resistors in series.
3. (Currently Amended) The A circuit of Claim 1, comprising:
  - a) a differential signal transmission line;
  - b) a common mode circuit comprising first and second resistances in series, said common mode circuit in communication with said differential signal transmission line, configured to reduce a swing of said differential signal transmission line; and
  - c) at least one overvoltage protection circuit in communication with said common mode circuit, wherein at least part of said common mode circuit is electrically interposed between said overvoltage protection circuit and said differential signal transmission line and said overvoltage protection circuit is coupled to a node between said first and second resistances.

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4. (Previously Presented) The circuit of Claim 1, wherein said first and second resistances comprise first and second termination resistors.
5. (Previously Presented) The circuit of Claim 1, further comprising an input buffer configured to receive a differential signal from said differential signal transmission line.
6. (Previously Presented) The circuit of Claim 5, wherein each of said first and second resistances is less than a resistance component of an impedance of said input buffer.
7. (Previously Presented) The circuit of Claim 1, wherein said common mode circuit further comprises a third resistor configured to receive a common mode voltage.
8. (Previously Presented) The circuit of Claim 7, wherein said third resistor is coupled to a node between said first and second resistances.
9. (Currently Amended) The A circuit of Claim 1, comprising:
  - a) a differential signal transmission line;
  - b) a common mode circuit comprising first and second resistances in series and a third resistor coupled to a node between said first and second resistances, said third resistor configured to receive a common mode voltage, and said common mode circuit in communication with said differential signal transmission line and configured to reduce a swing of said differential signal transmission line; and
  - c) at least one overvoltage protection circuit in communication with said common mode circuit, wherein at least part of said common mode circuit is electrically interposed between said overvoltage protection circuit and said differential signal transmission line and said overvoltage protection circuit is also coupled to said node between said first and second resistances.

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10. (Previously Presented) The circuit of Claim 8, wherein said third resistor has a resistance at least ten times greater than a resistance of said first and second resistances.
11. (Previously Presented) The circuit of Claim 10, wherein said third resistor has a resistance at least one hundred times greater than said resistance of said first and second resistances.
12. (Original) The circuit of Claim 1, further comprising first and second input terminals configured to receive a differential signal for said differential signal transmission line.
13. (Original) The circuit of Claim 1, wherein said differential signal transmission line comprises a first conduit and a second conduit, wherein said second conduit is complementary to said first conduit.
14. (Currently Amended) ~~The A circuit of Claim 18, comprising:~~
  - a) a differential signal transmission line;
  - b) ~~wherein said a common mode circuit in communication with said differential signal transmission line, comprising~~comprises first and second resistors in series between said first and second conduits, and configured to reduce a swing of said differential signal transmission line; and
  - c) ~~said an overvoltage protection circuit is coupled to a node between said first and second resistors, comprising at least one diode in communication with said common mode circuit, wherein said at least one diode has a threshold voltage greater than a voltage swing of said differential signal transmission line and at least part of said common mode circuit is electrically interposed between said diode and said differential signal transmission line.~~
15. (Previously Presented) The circuit of Claim 18, wherein said differential signal transmission line has a maximum voltage swing of less than 2 volts.

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16. (Previously Presented) The circuit of Claim 15, wherein said differential signal transmission line has a maximum voltage swing of less than 1.5 volts.
17. (Original) The circuit of Claim 1, wherein said at least one overvoltage protection circuit comprises at least one diode.
18. (Previously Presented) A circuit, comprising:
  - a) a differential signal transmission line;
  - b) a common mode circuit in communication with said differential signal transmission line, configured to reduce a swing of said differential signal transmission line; and
  - c) at least one diode in communication with said common mode circuit, wherein said at least one diode has a threshold voltage greater than a voltage swing of said differential signal transmission line and at least part of said common mode circuit is electrically interposed between said diode and said differential signal transmission line.
19. (Original) The circuit of Claim 17, wherein said at least one overvoltage protection circuit comprises at least two diodes in series.
20. (Original) The circuit of Claim 1, wherein said at least one overvoltage protection circuit is in further communication with a low impedance node.
21. (Original) The circuit of Claim 20, wherein said low impedance node comprises a power supply node, a virtual ground node or a ground potential.
22. (Currently Amended) The A circuit of Claim 4, comprising:
  - a) a differential signal transmission line;

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- b) wherein said a common mode circuit further comprises comprising first and second termination resistors in series, and third and fourth resistors in series between said first and second termination resistors, said common mode circuit in communication with said differential signal transmission line, configured to reduce a swing of said differential signal transmission line; and
  - c) at least one overvoltage protection circuit in communication with said common mode circuit, wherein at least part of said common mode circuit is electrically interposed between said overvoltage protection circuit and said differential signal transmission line.
23. (Original) The circuit of Claim 22, wherein said at least one overvoltage protection circuit comprises (i) a first overvoltage protection circuit coupled to a first node between said first termination resistor and said third resistor, and (ii) a second overvoltage protection circuit coupled to a second node between said second termination resistor and said fourth resistor.
24. (Original) A circuit, comprising:
- a) means for transferring a differential signal;
  - b) means for reducing a swing of said means for transferring; and
  - c) at least one means for protecting circuitry to which said differential signal is to be transferred from an overvoltage, wherein at least part of said means for reducing is electrically interposed between said at least one means for protecting and said means for transferring.
25. (Original) The circuit of Claim 24, wherein said means for reducing comprises first and second resistors in series.
26. (Currently Amended) The A circuit of Claim 25, comprising:
- a) means for transferring a differential signal;

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- b) means for reducing a swing of said means for transferring; and
  - c) wherein-said at least one means for protecting circuitry to which said differential signal is to be transferred from an overvoltage is coupled to a node between said first and second resistors, wherein at least part of said means for reducing is electrically interposed between said at least one means for protecting and said means for transferring.
27. (Original) The circuit of Claim 25, further comprising a means for buffering said differential signal, configured to receive said differential signal from said means for transferring.
28. (Original) The circuit of Claim 27, wherein said first and second resistors each have a resistance less than a resistance component of an impedance of said means for buffering.
29. (Original) The circuit of Claim 24, wherein said means for reducing comprises a means for applying a common mode voltage.
30. (Original) The circuit of Claim 29, wherein said means for applying is coupled to a node between first and second means for terminating said differential signal.
31. (Original) The circuit of Claim 29, wherein said means for applying a common mode voltage comprises a resistor receiving said common mode voltage.
32. (Original) The circuit of Claim 31, wherein said resistor has a resistance at least one hundred times greater than said resistance of said first and second means for terminating.
33. (Currently Amended) ~~The A circuit of Claim 32, comprising:~~  
a) means for transferring a differential signal;

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- b) a means for applying a common mode voltage, comprising a resistor receiving said common mode voltage and having a resistance at least one hundred times greater than a resistance of first and second means for terminating said differential signal; and
  - c) wherein said at least one means for protecting circuitry to which said differential signal is to be transferred from an overvoltage is also coupled to said a node between said first and second means for terminating, wherein at least part of said means for applying is electrically interposed between said at least one means for protecting and said means for transferring.
34. (Original) The circuit of Claim 24, wherein said means for transferring comprises a differential signal transmission line.
35. (Original) The circuit of Claim 34, further comprising means for receiving said differential signal for said differential signal transmission line.
36. (Original) The circuit of Claim 34, wherein said differential signal transmission line comprises a first conduit and a second conduit, wherein said second conduit is complementary to said first conduit.
37. (Currently Amended) The A circuit of Claim 36, comprising:
- a) means for transferring a differential signal;
  - b) wherein said means for reducing a swing of said means for transferring, comprises comprising first and second resistors in series between said first and second conduits[.]; and
  - c) said at least one means for protecting circuitry to which said differential signal is to be transferred from an overvoltage is coupled to a node between said first and second resistors, wherein at least part of said means for reducing is electrically

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interposed between said at least one means for protecting and said means for transferring.

38. (Original) The circuit of Claim 24, wherein said means for transferring has a maximum voltage swing of less than 2 volts.
39. (Original) The circuit of Claim 24, wherein said at least one means for protecting comprises at least one diode.
40. (Original) The circuit of Claim 39, wherein said at least one diode has a threshold voltage greater than a voltage swing of said means for transferring.
41. (Original) The circuit of Claim 26, wherein said at least one means for protecting is in further communication with a low impedance node.
42. (Currently Amended) ~~The~~ A circuit of Claim 25, comprising:  
a) means for transferring a differential signal;  
b) ~~wherein said means for reducing~~ a swing of said means for transferring, comprising first and second resistors in series and further comprises third and fourth resistors in series between said first and second resistors; and  
c) at least one means for protecting circuitry to which said differential signal is to be transferred from an overvoltage, wherein at least part of said means for reducing is electrically interposed between said at least one means for protecting and said means for transferring.
43. (Original) The circuit of Claim 42, wherein said at least one means for protecting comprises (i) a first means for protecting coupled to a first node between said first and third resistors, and (ii) a second means for protecting coupled to a second node between said second and fourth resistors.



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44. (Original) An integrated circuit, comprising:
- a) first and second input terminals configured to receive a differential signal;
  - b) an input buffer configured to receive said differential signal; and
  - c) the circuit of Claim 1, wherein said differential signal transmission line communicates said differential signal from said input terminals to said input buffer.
45. (Canceled)
46. (Currently Amended) ~~The~~ An integrated circuit of Claim 44, comprising:
- a) first and second input terminals configured to receive a differential signal;
  - b) an input buffer configured to receive said differential signal; and
  - c) a circuit, comprising:
    - i) a differential signal transmission line configured to communicate said differential signal from said input terminals to said input buffer;
    - ii) a common mode circuit comprising first and second resistances in series, said common mode circuit in communication with said differential signal transmission line, configured to reduce a swing of said differential signal transmission line; and
    - iii) wherein said at least one overvoltage protection circuit is coupled to a node between said first and second resistances and in communication with said common mode circuit, wherein at least part of said common mode circuit is electrically interposed between said overvoltage protection circuit and said differential signal transmission line.
47. (Previously Presented) The integrated circuit of Claim 44, wherein each of said first and second resistances is less than a resistance component of an impedance of said input buffer.

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48. (Previously Presented) The integrated circuit of Claim 44, wherein said common mode circuit further comprises a third resistor configured to receive a common mode voltage.
49. (Previously Presented) The integrated circuit of Claim 48, wherein said third resistor is coupled to a node between said first and second resistances.
50. (Previously Presented) The integrated circuit of Claim 48, wherein said third resistor has a resistance at least one hundred times greater than said resistance of said first and second resistances.
51. (Original) The integrated circuit of Claim 44, wherein said differential signal transmission line comprises a first conduit and a second conduit, wherein said second conduit is complementary to said first conduit.
52. (Canceled)
53. (Original) The integrated circuit of Claim 44, wherein said differential signal transmission line has a maximum voltage swing of less than 2 volts.
54. (Original) The integrated circuit of Claim 44, wherein said at least one overvoltage protection circuit comprises at least one diode.
55. (Canceled)
56. (Original) The integrated circuit of Claim 44, further comprising first and second input pins respectively coupled to said first and second input terminals and configured to receive an external differential signal.

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57. (Original) The integrated circuit of Claim 44, wherein said at least one overvoltage protection circuit is in further communication with a low impedance node.
58. (Original) The integrated circuit of Claim 57, wherein said low impedance node comprises a power supply node, a virtual ground node or a ground potential.
59. (Currently Amended) ~~The~~ An integrated circuit of Claim 44, comprising:  
a) first and second input terminals configured to receive a differential signal;  
b) an input buffer configured to receive said differential signal; and  
c) a circuit, comprising:  
i) a differential signal transmission line configured to communicate said differential signal from said input terminals to said input buffer;  
ii) wherein said a common mode circuit comprising first and second resistances in series, and further comprises third and fourth resistors in series between said first and second resistances, said common mode circuit in communication with said differential signal transmission line, configured to reduce a swing of said differential signal transmission line; and  
iii) at least one overvoltage protection circuit in communication with said common mode circuit, wherein at least part of said common mode circuit is electrically interposed between said overvoltage protection circuit and said differential signal transmission line.
60. (Previously Presented) The integrated circuit of Claim 59, wherein said at least one overvoltage protection circuit comprises (i) a first overvoltage protection circuit coupled to a first node between said first resistance and said third resistor, and (ii) a second overvoltage protection circuit coupled to a second node between said second resistance and said fourth resistor.

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61. (Original) A system for transferring data on or across a network, comprising:
- a) the integrated circuit of Claim 44;
  - b) at least one transmitter communicatively coupled to said first and second input terminals, said transmitter being configured to transmit a differential data signal; and
  - c) at least one receiver communicatively coupled to said input buffer, said receiver being configured to receive said differential data signal.
62. (Original) The system of Claim 61, wherein said integrated circuit further comprises said receiver.
63. (Previously Presented) A network, comprising:
- a) a plurality of systems, communicatively coupled to each other, each system comprising:
    - i) an integrated circuit, comprising first and second input terminals configured to receive a differential signal, an input buffer configured to receive said differential signal, and a circuit, comprising (i) a differential signal transmission line configured to communicate said differential signal from said input terminals to said input buffer, (ii) a common mode circuit in communication with said differential signal transmission line, configured to reduce a swing of said differential signal transmission line, and (iii) at least one overvoltage protection circuit in communication with said common mode circuit, wherein at least part of said common mode circuit is electrically interposed between said overvoltage protection circuit and said differential signal transmission line;
    - ii) at least one transmitter communicatively coupled to said first and second input terminals, said transmitter being configured to transmit a differential data signal; and

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- iii) at least one receiver communicatively coupled to said input buffer, said receiver being configured to receive said differential data signal; and
  - b) a plurality of storage or communications devices, each of said storage or communications devices being communicatively coupled to one of said systems.
64. (Original) The network of Claim 63, wherein each of said storage or communications devices comprises a storage device.
65. (Original) An integrated circuit, comprising:
- a) means for receiving a differential signal;
  - b) means for buffering said differential signal; and
  - c) the circuit of Claim 24, wherein said means for transferring communicates said differential signal from said means for receiving to said means for buffering.
66. (Original) The integrated circuit of Claim 65, wherein said means for reducing comprises first and second means for terminating said differential signal.
67. (Currently Amended) ~~The~~ An integrated circuit of Claim 66, comprising:
- a) means for receiving a differential signal;
  - b) means for buffering said differential signal; and
  - c) a circuit, comprising:
    - i) means for transferring a differential signal that communicates said differential signal from said means for receiving to said means for buffering;
    - ii) means for reducing a swing of said means for transferring, comprising first and second means for terminating said differential signal; and
    - iii) wherein said at least one means for protecting circuitry to which said differential signal is to be transferred from an overvoltage is coupled to a node between said first and second means for terminating, wherein at least

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part of said means for reducing is electrically interposed between said at least one means for protecting and said means for transferring.

68. (Original) The integrated circuit of Claim 66, wherein said first and second means for terminating each comprise a resistor having a resistance less than a resistance component of an impedance of said means for buffering.
69. (Original) The integrated circuit of Claim 66, wherein said means for reducing comprises a resistor configured to receive a common mode voltage.
70. (Original) The integrated circuit of Claim 69, wherein said resistor is coupled to a node between said first and second means for terminating.
71. (Currently Amended) ~~The~~ An integrated circuit of Claim 70, comprising:
- a) means for receiving a differential signal;
  - b) means for buffering said differential signal; and
  - c) a circuit comprising:
    - i) means for transferring a differential signal that communicates said differential signal from said means for receiving to said means for buffering;
    - ii) means for reducing a swing of said means for transferring, comprising first and second means for terminating said differential signal and a resistor configured to receive a common mode voltage coupled to a node between said first and second means for terminating; and
    - iii) wherein said at least one means for protecting circuitry to which said differential signal is to be transferred from an overvoltage is also coupled to said node between said first and second means for terminating, wherein at least part of said means for reducing is electrically interposed between said at least one means for protecting and said means for transferring.

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72. (Original) The integrated circuit of Claim 70, wherein said resistor has a resistance at least one hundred times greater than a resistance of said first and second means for terminating.
73. (Original) The integrated circuit of Claim 65, wherein said means for transferring comprises a first conduit and a second conduit, wherein said second conduit is complementary to said first conduit.
74. (Currently Amended) ~~The~~ An integrated circuit of ~~Claim 73~~, comprising:
- a) means for receiving a differential signal;
  - b) means for buffering said differential signal; and
  - c) a circuit, comprising:
    - i) means for transferring a differential signal that communicates said differential signal from said means for receiving to said means for buffering, comprising a first conduit and a second conduit, wherein said second conduit is complementary to said first conduit;
    - ii) ~~wherein said means for reducing a swing of said means for transferring,~~ comprises comprising first and second means for terminating said differential signal in series between said first and second conduits[.]; and
    - iii) said at least one means for protecting circuitry to which said differential signal is to be transferred from an overvoltage is coupled to a node between said first and second resistors means for terminating.
75. (Original) The integrated circuit of Claim 65, wherein means for transferring has a maximum voltage swing of less than 2 volts.
76. (Original) The integrated circuit of Claim 65, wherein said at least one means for protecting comprises at least one diode.

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77. (Original) The integrated circuit of Claim 76, wherein said at least one diode has a threshold voltage greater than a voltage swing of said means for transferring.
78. (Original) The integrated circuit of Claim 65, further comprising means for receiving an external differential signal coupled to said means for transferring.
79. (Original) The integrated circuit of Claim 65, wherein said at least one means for protecting is in communication with a low impedance node.
80. (Original) The integrated circuit of Claim 67, wherein said means for reducing further comprises first and second resistors in series between said first and second means for terminating.
81. (Original) The integrated circuit of Claim 80, wherein said at least one means for protecting comprises (i) a first means for protecting coupled to a first node between said first means for terminating and said first resistor, and (ii) a second means for protecting coupled to a second node between said second means for terminating and said second resistor.
82. (Original) A system for transferring data on or across a network, comprising:
- a) the integrated circuit of Claim 65;
  - b) at least one means for transmitting a differential data signal, communicatively coupled to said means for transferring; and
  - c) at least one means for receiving said differential data signal, communicatively coupled to said means for buffering.
83. (Original) The system of Claim 82, wherein said integrated circuit further comprises said means for receiving.



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84. (Original) A network, comprising:
- a) a plurality of the systems of Claim 82, communicatively coupled to each other; and
  - b) a plurality of means for storing or communicating, each of said means for storing or communicating being communicatively coupled to one of said systems.
85. (Original) The network of Claim 84, wherein each of said means for storing or communicating comprises a means for storing.
86. (Original) A method of protecting a differential circuit from an overvoltage, comprising the steps of:
- a) receiving a differential signal in said differential circuit;
  - b) controlling a voltage swing of said differential signal with a termination circuit in communication with said differential circuit; and
  - c) when said differential circuit receives said overvoltage, shunting said overvoltage to a low impedance node through said termination circuit, and otherwise, processing said differential signal through circuitry coupled to said differential circuit.
87. (Original) The method of Claim 86, wherein said shunting comprises passing said overvoltage through at least one diode.
88. (Original) The method of Claim 86, wherein said low impedance node comprises a power supply node, a virtual ground node or a ground potential.
89. (Currently Amended) The method of Claim ~~88~~86, wherein said shunting comprises passing said overvoltage through at least one diode.

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90. (Original) The method of Claim 86, wherein said termination circuit comprises first and second resistors having a common mode node therebetween.
91. (Original) The method of Claim 90, wherein said controlling step comprises applying a common mode voltage to said common mode node.
92. (Original) The method of Claim 91, wherein said common mode voltage is applied to said common mode node through a resistor having a resistance greater than a resistance component of an impedance of said circuitry.
93. (Original) The method of Claim 92, further comprising the step of generating said common mode voltage.
94. (Original) The method of Claim 86, wherein said processing comprises buffering said differential signal.
95. (Original) The method of Claim 86, wherein said differential circuit comprises (i) first and second input pads and (ii) a differential signal transmission line electrically coupled to said first and second input pads.
96. (Original) The method of Claim 95, wherein said termination circuit comprises a first resistor coupled to a first conduit of said differential signal transmission line, a second resistor coupled to a second conduit of said differential signal transmission line, and a common mode node between said first and second resistors, wherein said second conduit is complementary to said first conduit.
97. (Previously Presented) The circuit of Claim 1, wherein said differential signal transmission line has a maximum voltage swing of less than 2 volts.

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98. (Previously Presented) The circuit of Claim 97, wherein said differential signal transmission line has a maximum voltage swing of less than 1.5 volts.
99. (Previously Presented) The circuit of Claim 18, further comprising an input buffer configured to receive a differential signal from said differential signal transmission line, and said common mode circuit comprises first and second resistances in series.
100. (Previously Presented) The circuit of Claim 99, wherein each of said first and second resistances is less than a resistance component of an impedance of said input buffer.
101. (Previously Presented) The circuit of Claim 99, wherein said common mode circuit further comprises a third resistance configured to receive a common mode voltage.
102. (Currently Amended) ~~The A circuit of Claim 101,~~ comprising:
- a) a differential signal transmission line;
  - b) an input buffer configured to receive a differential signal from said differential signal transmission line;
  - c) a common mode circuit in communication with said differential signal transmission line, configured to reduce a swing of said differential signal transmission line and comprising first and second resistances in series and a third resistance configured to receive a common mode voltage; and
  - d) wherein said an overvoltage protection circuit is comprising at least one diode in communication with said common mode circuit and coupled to a node between said first and second resistances, wherein said at least one diode has a threshold voltage greater than a voltage swing of said differential signal transmission line and at least part of said common mode circuit is electrically interposed between said diode and said differential signal transmission line.

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103. (Previously Presented) The circuit of Claim 101, wherein said third resistance is at least ten times greater than said first and second resistances.
104. (Previously Presented) The circuit of Claim 103, wherein said third resistance is at least one hundred times greater than said first and second resistances.
105. (Previously Presented) An integrated circuit, comprising:
- a) first and second input terminals configured to receive a differential signal;
  - b) an input buffer configured to receive said differential signal; and
  - c) the circuit of Claim 18, wherein said differential signal transmission line communicates said differential signal from said input terminals to said input buffer.
106. (Previously Presented) The integrated circuit of Claim 105, wherein said common mode circuit comprises first and second resistances in series, wherein each of said first and second resistances is less than a resistance component of an impedance of said input buffer.
107. (Previously Presented) The integrated circuit of Claim 105, wherein said common mode circuit further comprises a third resistance configured to receive a common mode voltage.
108. (Previously Presented) The integrated circuit of Claim 107, wherein said third resistance is coupled to a node between said first and second resistances.
109. (Previously Presented) The integrated circuit of Claim 107, wherein said third resistance is at least ten times greater than said first and second resistances.
110. (Previously Presented) The integrated circuit of Claim 109, wherein said third resistance is at least one hundred times greater than said first and second resistances.

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111. (Previously Presented) The network of Claim 63, wherein said common mode circuit comprises first and second resistances in series.
112. (Previously Presented) The network of Claim 111, wherein each of said first and second resistances is less than a resistance component of an impedance of said input buffer.
113. (Previously Presented) The network of Claim 111, wherein said common mode circuit further comprises a third resistance configured to receive a common mode voltage.
114. (Currently Amended) The A network of Claim 113, comprising:
- a) a plurality of systems, communicatively coupled to each other, each system comprising:
- i) an integrated circuit, comprising first and second input terminals configured to receive a differential signal, an input buffer configured to receive said differential signal, and a circuit, comprising (i) a differential signal transmission line configured to communicate said differential signal from said input terminals to said input buffer, (ii) a common mode circuit in communication with said differential signal transmission line, configured to reduce a swing of said differential signal transmission line and comprising first and second resistances in series and a third resistance configured to receive a common mode voltage, and (iii) wherein said at least one overvoltage protection circuit in communication with said common mode circuit and is coupled to a node between said first and second resistances, wherein at least part of said common mode circuit is electrically interposed between said overvoltage protection circuit and said differential signal transmission line, and said third resistance is at least ten times greater than said first and second resistances;

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- ii) at least one transmitter communicatively coupled to said first and second input terminals, said transmitter being configured to transmit a differential data signal; and
  - iii) at least one receiver communicatively coupled to said input buffer, said receiver being configured to receive said differential data signal; and
  - b) a plurality of storage or communications devices, each of said storage or communications devices being communicatively coupled to one of said systems.
115. (Previously Presented) The network of Claim 114, wherein said third resistance is at least one hundred times greater than said first and second resistances.
116. (Previously Presented) The network of Claim 63, wherein said differential signal transmission line has a maximum voltage swing of less than 2 volts.
117. (Previously Presented) The network of Claim 116, wherein said differential signal transmission line has a maximum voltage swing of less than 1.5 volts.
118. (Previously Presented) The network of Claim 63, wherein said at least one overvoltage protection circuit comprises at least one diode.
119. (Previously Presented) The network of Claim 118, wherein said at least one diode has a threshold voltage greater than a voltage swing of said differential signal transmission line.
120. (Previously Presented) A circuit, comprising:
- a) a differential input signal;
  - b) a voltage divider in communication with said differential input signal, configured to reduce a swing of said differential signal transmission line; and

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- c) a common mode voltage and at least one overvoltage protection circuit coupled to a node in said voltage divider.

121. (Previously Presented) A circuit, comprising:

- a) a differential input signal;
- b) a voltage divider in communication with said differential input signal, configured to reduce a swing of said differential signal transmission line;
- c) a common mode voltage coupled to a first node in said voltage divider;
- d) a first overvoltage protection circuit coupled to a second node in said voltage divider; and
- e) a second overvoltage protection circuit coupled to a third node in said voltage divider, said first node being between said second and third nodes.